Attorney Docket No. NSC1-P300/P05882

PATENT APPLICATION

WAFER LEVEL PACKAGE DESIGN THAT FACILITATES TRIMMING AND TESTING

Inventor:

Nikhil Vishwanath Kelkar
6385 Lillian Way
San Jose, CA 95120

Assignee:
National Semiconductor Corporation

Prepared by:

BEYER, WEAVER & THOMAS, LLP
P.O. Box 778
Berkeley, CA 94704-0778

WAFER LEVEL PACKAGE DESIGN THAT FACILITATES TRIMMING AND TESTING

BACKGROUND

[0001] The present invention relates generally wafer level processing of integrated circuits. More particularly, a wafer level packaging arrangement is described that permits parameter trimming and final testing to be accomplished during a single probing sequence.

[0002] A variety of semiconductor devices (particularly precision analog semiconductor devices) require that the circuits be trimmed after fabrication. Generally, trimming is the process of fine-tuning the performance of an integrated circuit device after fabrication in order to ensure conformance to a desired performance specification. In order to facilitate trimming, it is common to provide metal pads, often referred to as "trim pads" on the active surface of the die. Generally, a specific current is applied to each trim pad at a specific voltage in order to activate components (e.g. fuses) that can adjust the performance of the circuits of interest.

[0003] There are a number of conventional processes for packaging integrated circuits. One approach that is commonly referred to as "flip chip" packaging generally contemplates forming solder bumps (or other suitable contacts) directly on the face of an integrated circuit die. In some situations, the contacts are formed directly on I/O pads formed on the die, whereas in other situations the contacts are redistributed. The die is then typically attached to a substrate such as a printed circuit board or a package substrate such that the die contacts directly connect to corresponding contacts on the substrate.

[0004] When trim pads are included in flip chip package designs (or other wafer level chip scale packages) it is common to deposit a passivation material over the trim pads after the device has been trimmed. By way of example, a representative process might proceed as illustrated in Figure 5. Specifically, after the wafer is fabricated (302), the wafer is taken to a wafer prober which tests and trims the appropriate

circuits (304). The trim pads are generally formed from aluminum and thus they will corrode if left exposed in an ambient environment. Also, if they are left exposed when the singulated die is soldered to a substrate, there is a significant risk that the solder may bridge the gap between one of the bond pad/trim pad pairs, thereby shorting out the die. To avoid these problems, some manufacturing approaches contemplate covering the trim pads with a passivation material after the wafer has been trimmed. This helps reduce corrosion of the trim pads but requires returning to the wafer to the wafer processing chamber where a passivation layer (e.g. polyimide or benzocyclobutene (BCB)) is applied over the trim pads (306). Typically, the passivation layer also extends over edge portions of the I/O pads as well. Thus, the passivation layer is used to isolate the trim pads.

[0005] After the passivation layer is applied, appropriate underbump metallization stacks are typically formed on the I/O pads (308) and the wafer is bumped (310). It should be appreciated that there may be a number of other processing steps that occur before, as part of, or after the bumping. When the desired processing is completed, the wafer is again taken to a wafer prober where the final testing occurs.

[0006] In this scenario, wafer probe testing must be done twice. Initially, the wafer must be probed to facilitate trimming, which must occur before the trim pads are insulated by the passivation material. The wafer must also be probed a second time to test for electrical function after the contact bumps have been placed on the dies. Although the described process works well, this two-part wafer probing process is inefficient, since the wafer must go to a testing facility for trimming, and subsequently, to a manufacturing facility to cover the trim pads and then back to the testing facility for the final wafer probing before the dies are cut and shipped to customers. These inefficiencies add to the overall cost of manufacturing these IC devices. Therefore, there are continuing efforts to reduce the costs and time associated with the manufacturing process.

SUMMARY

[0007] To achieve the foregoing and other objects of the invention, a wafer level method of packaging, trimming and testing integrated circuits is described. In a method aspect of the invention, a wafer having trim pads is bumped before the wafer is trimmed. After the bumping, the dice on the wafer are trimmed and tested using standard trim probing and test probing approaches. After the trimming and testing, an electrically insulative undercoating is applied to the active surface of the wafer. The undercoating directly covers the trim pads while leaving at least portions of the contact bumps exposed. With this approach, the wafer may be trimmed and tested at substantially the same stage of wafer processing. The trimming and testing operations may be performed either sequentially or substantially simultaneously.

[0008] The undercoating may be applied using a variety of different processes, including spin-on coating, molding, screen printing or stencil printing. The undercoating may be formed from a wide variety of material including epoxy, polyimide and silicone-polyimide copolymers. In some specific applications, it may be desirable to utilize a curable material (such as an epoxy material) to form the undercoating or even a B-stageable material. In some embodiments, the undercoating may even be arranged to act as an underfill.

[0009] The resulting wafers and integrated circuits do not have a passivation layer that extends over the trim pads. Rather, the undercoating electrically isolates the trim pads. In some applications, the undercoating may have a thickness in the range of approximately 0.2 and 4 mils.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The invention, together with further objects and advantages thereof, may best be understood by reference to the following description taken in conjunction with the accompanying drawings in which:

FIG. 1(a) illustrates in top plan view an exemplary wafer that has been formed in accordance with an embodiment the present invention.

FIG. 1(b) illustrates in top perspective view a surface mount semiconductor die scribed from the wafer of FIG. 1.

FIG. 2(a) is a diagrammatic cross sectional view of a portion of a wafer prior to bumping.

FIG. 2(b) is a diagrammatic cross sectional view of the portion of a wafer illustrated in Fig. 2(a) after bumping and undergoing simultaneous testing and trim probing in accordance with an embodiment of the present invention.

FIG. 3 is a diagrammatic cross sectional view of the portion of a wafer illustrated in Fig 2(b) after application of an undercoat in accordance with an embodiment of the present invention.

FIG. 4 is a process flow diagram illustrating a method of packaging, trimming and testing a wafer in accordance with one embodiment of the present invention.

FIG. 5 is a process flow diagram illustrating an earlier method of packaging, trimming and testing a wafer.

[0011] It is to be understood that, in the drawings, like reference numerals designate like structural elements. Also, it is understood that the depictions in the figures are diagrammatic in nature and not to scale.

DETAILED DESCRIPTION

[0012] In the described embodiments, a wafer is bumped prior to trimming. The bumped wafer may then be trimmed and final tested at substantially the same stage of wafer processing. The dice on the wafer are trimmed and tested using standard trim probing and test probing approaches. After the trimming and testing, an electrically insulative undercoating is applied to the active surface of the wafer. The undercoating directly covers the trim pads while leaving at least portions of the contact bumps exposed.

[0013] Referring initially to Fig. 4 in conjunction with Fig. 2(a), a method of fabricating a wafer in accordance with one embodiment of the invention will be described. Initially, a wafer 100 is fabricated using conventional and/or appropriate wafer fabrication techniques (400). As will be appreciated by those skilled in the art, there are a wide variety of suitable wafer fabrication techniques. The wafer generally will include a multiplicity of dice 102, which each include a number of I/O pads 103 and trim pads 105. Fig. 2(a) diagrammatically illustrates what a cross section of a suitable wafer might look like. Of particular note, a passivation layer 107 generally covers the top surface of the wafer. However, the passivation layer 107 has opening that expose the I/O pads 103 and trim pads 105.

[0014] When solder bumps are to be formed directly on the die, it is often desirable to form underbump metallization (UBM) stacks 110 over the I/O pads 103 to provide a good / non-corrosive adhesion base for the solder bumps. (Step 402). In the illustrated embodiment, corresponding metallization stacks 108 are also formed over the trim pads 105. When the trim pads 105 are formed from a material (e.g. aluminum) that oxidizes when exposed to air, it can be particularly advantageous to metalize the trim pads 105 in addition to the I/O pads 103. However, it should be appreciated that the trim pads could alternatively be masked so that the metallization stacks 108 are eliminated. After the underbump metallization stacks 110 have been formed, the wafer may be bumped by any of a wide variety of bumping processes (404). Typically, bumping involves forming solder balls on the underbump metallization stacks, however other suitable contact bump formation techniques (including non-solder based bump formation) can be used as well.

[0015] A representative resulting bumped wafer 100 is illustrated in Fig. 1. As seen therein, the representative wafer 100 includes a plurality of dice 102. Each of the dice 102 includes a plurality of solder balls, contacts or "bumps" 106 that are intended to be mounted directly onto contact pads of a substrate, such as a printed circuit board (PCB). The bumps 106 may be formed on the metallization stacks 108 as described above, directly on I/O pads on the die or redistributed using conventional redistribution techniques. (In the case of redistribution, if desired, the trim pads could also be redistributed). It should be noted that while only a relatively small number of dice 102 are shown on the wafer 100 for purposes of illustration, most wafers have significantly more dice formed thereon. By way of example, current state of the art wafers typically have several hundred to several thousand dice formed thereon, and some have more than ten thousand dice. As is well known in the art, most wafers and dice are formed of silicon, although any other appropriate semiconductor material can also be used, including, for example, gallium arsenide (GaAs), indium gallium phosphide, silicon germanium, and the like.

[0016] After the wafer has been bumped, other desired wafer level processing such as applying an opaque backcoating to the back surface of the wafer, wafer thinning, marking the wafer, etc. may be performed as desired (406). After the other desired wafer processing (if any) is performed, the wafer is trimmed and final tested (410). The trimming and final testing may be performed either sequentially (i.e., using two or more passes of the wafer prober) or simultaneously (i.e., using a single pass of the wafer prober). The step of wafer probing is diagrammatically illustrated in Fig. 2(b).

[0017] After the testing, an undercoating is applied to the active surface of the wafer (412). The structure of a representative wafer 100 having an undercoating 130 formed thereon is diagrammatically illustrated in Fig. 3. The undercoating 130 may be formed from a wide variety of materials. By way of example, a wide variety of polymer based materials including epoxies, polyimides, silicone-polymide copolymers or BCB work well. The undercoating can be applied using any of a variety of conventional coating techniques, including spin-on coating processes, molding processes, screen printing processes, stencil printing processes, etc. The important point is that an undercoating is used as opposed to a conventional

semiconductor passivation material such as silicon-nitride or silicon-oxide. As will be appreciated by those skilled in the art, the deposition of a passivation material would require reintroduction of the wafer into a deposition chamber, whereas the simple application of an undercoating does not.

[0018] The described undercoating covers the trim pads thereby both electrically insulating the trim pads and isolating the trim pads from the surrounding environment (thereby lowering the risk of corrosion). Since the application of the undercoating (as well as any other wafer processing that occurs after the testing/trimming step is not expected, intended or likely to affect the electrical characteristics of the integrated circuits in any significant manner, there is generally no need to retest the dice at the wafer level after the undercoating has been applied. This is a significant advantage over approaches where the wafer is passivated and bumped after trimming. In those situations, it is generally considered necessary and important to retest the wafer after the passivation and bumping processes have been completed.

[0019] It should be appreciated that there are a number of existing processes that contemplate the application of an undercoating to the active surface of a wafer for a variety of different reasons. In many applications, the undercoating 130 used in the present invention may perform multiple functions including some of the functions performed by existing undercoatings. By way of example, U.S. Patent Nos. 6,352,881 and 6,245,595 and pending application Nos. 10/080,913 and 10/224,291 (which are incorporated herein by reference) all describe the application of an underfill adhesive material to the front surface of the wafer. Some of the described embodiments utilize B-stageable materials (e.g. B-stageable epoxy materials) as the underfill material. If desired, the undercoating 130 may be an underfill material, as for example a B-stageable underfill material. It should be appreciated that generally, an underfill material is intended to fill the region between the die and a substrate that the die is mounted to after the wafer has been diced and the die mounted to the substrate. U.S. Patent Application No. 10/707,208 (which is incorporated herein by reference) describes the use of a hardened undercoat material to constrain the interface between solder balls and their associated contact pads. The undercoating 130 may advantageously be used for this purpose as well. Still other undercoatings and/or underfill adhesives are designed to be optically opaque in order to protect the front

surface of a die from exposure to light. Again, it should be appreciated that the undercoating 130 may be optically opaque to accomplish this function as well.

[0020] The thickness of the undercoating 130 may be varied widely depending on the needs of a particular situation. Typically undercoatings utilized as underfill materials will be thicker than undercoating that are not also used as underfill. In the illustrated embodiment, the undercoating (which is not used as an underfill) has a final thickness in the range of approximately 0.2 and 4 mils. In some applications, thicknesses in the range of 0.3 to 2 mils work well.

[0021] In the illustrated embodiment, the undercoating is formed from a curable material such as an epoxy resin. However, this is not a requirement. A wide variety of materials including thermosetting resins, thermoplastic materials, epoxies, polyimides, silicone-polymide copolymers may be used.

[0022] After the undercoating has been applied to the active surface of a wafer, then any additional wafer level processing that is desired may be performed, although it is generally preferable that only processes that are not expected to significantly impact the electrical characteristics of the integrated circuits be done after the wafer has been tested and trimmed. After any additional wafer level processing, the wafer may be singulated (414) using conventional wafer dicing techniques and the resulting dice may be handled as appropriate.

[0023] Although only a few embodiments of the invention have been described in detail, it should be appreciated that the invention may be implemented in many other forms without departing from the spirit or scope of the invention. In some circumstances, the ordering of the various described steps (and particularly the order of the other desired wafer processing steps) may be varied to suit the needs of a particular application. The undercoating coating may be formed from an opaque, partially opaque, a translucent or a transparent material.

[0024] In some embodiments, an opaque undercoating may be combined with a backcoating and/or wafer level side coating applications so that the dice are effectively encapsulated when they are singulated. The trim pads and contact pads may be formed from a wide variety of materials and/or stacks of materials. By way of example, common materials for use in the trim pads include aluminum, nickel, gold, copper, titanium, palladium, silver, chromium, tungsten and vanadium and various

alloys that include some of these materials. Therefore, the present embodiments are to be considered as illustrative and not restrictive and the invention is not to be limited to the details given herein, but may be modified within the scope and equivalents of the appended claims.